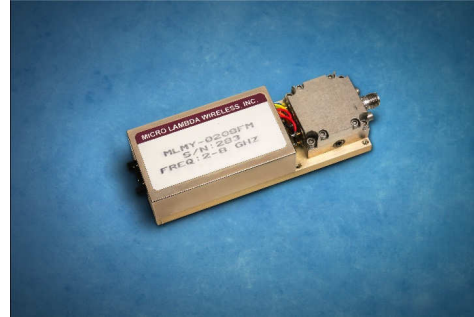


FEATURES

- 2 GHz To 22 GHz
- Compensation for Temperature Drift
- Voltage Regulators for Improved Stability
- 16 Bit Tuning Resolution


DESCRIPTION

Micro Lambda **MLPM and MLPW Series** Permanent Magnet YIG Oscillators are available with integrated serial driver circuits. These drivers eliminate the need for customers to design or develop their own driver circuits and sophisticated test and alignment procedures. Integrating a driver at Micro Lambda's factory ensures peak performance. Alignment and compensation with the particular YIG oscillator can be maximized down to the component level.

All drivers in this series provide input voltage regulators and compensation circuits to improve frequency drift. All voltages required by the YIG oscillator, except the heater inputs are supplied by the voltage regulators.

COMMERCIAL SERIAL DRIVERS	2-22 GHz PMO's, SD & SG SERIES
DRIVER INPUT & RESPONSE	SPECIFICATION (0 to +65 deg. C)
Tuning Command	Start Word (all 0's) = Lowest Frequency Stop Word (all 1's) = Highest Frequency
Tuning Resolution	16 BIT Positive Logic (Fmax-Fmin)/65,535 Bit Resolution
Tuning Accuracy (excluding hysteresis)	See Table (Page 3)
Tuning Speed (Note 1)	10 mS for 1 GHz step to within ± 10 MHz. (residual FM is 10 kHz Pk-Pk)
Main Driver Inputs	
Supply Voltage & Current (Note 2)	+12 V or +15 V $\pm .5$ V @ 265 mA, Max. -12 V or -15 V $\pm .5$ V @ 165 mA, Max.
Supply Voltage Pushing	± 100 kHz, Max. @ $\pm .5$ Vdc
Supply Voltage Ripple	10 mV Ripple Pk-Pk from 2 kHz to 3 MHz
Ground	Chassis Ground
YIG Heater Voltage & Current	+24 Vdc ± 4 Vdc @ 300 mA surge for 2 seconds, 25 mA steady state Polarity independent : ± 12 Vdc or ± 15 Vdc acceptable
Digital Interface	The MLWI digital driver interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE interfaces. The 3-wire serial interface will operate in a 5V or 3.3V logic system. The chip-select input (CSELECTn) frames the serial data loading at the data input pin (DATA). Immediately following CSELECTn's high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial-clock input (CLOCK). After 16 data bits have been loaded into the serial input register, it transfers its contents to the DAC latch on CSELECTn's low-to-high transition (Figure 2). Note that if CSELECTn does not remain low during the entire 16 CLOCK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

SD-SERIES — CONT.

Permanent Magnet Oscillators with Serial Drivers

Power-On Reset

The MLWI digital driver has a power-on reset circuit to set the DAC's output to OV(F-min) in unipolar mode when VDD is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after power loss.

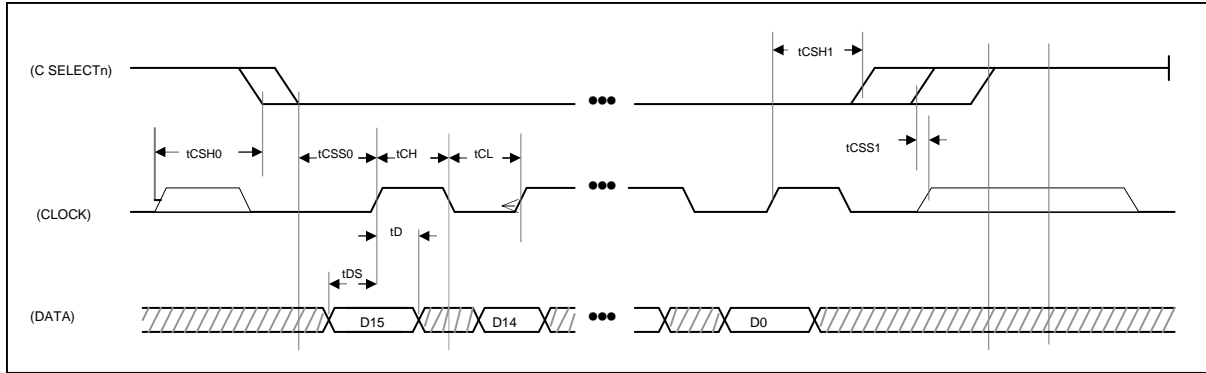


Figure 1. Timing Diagram

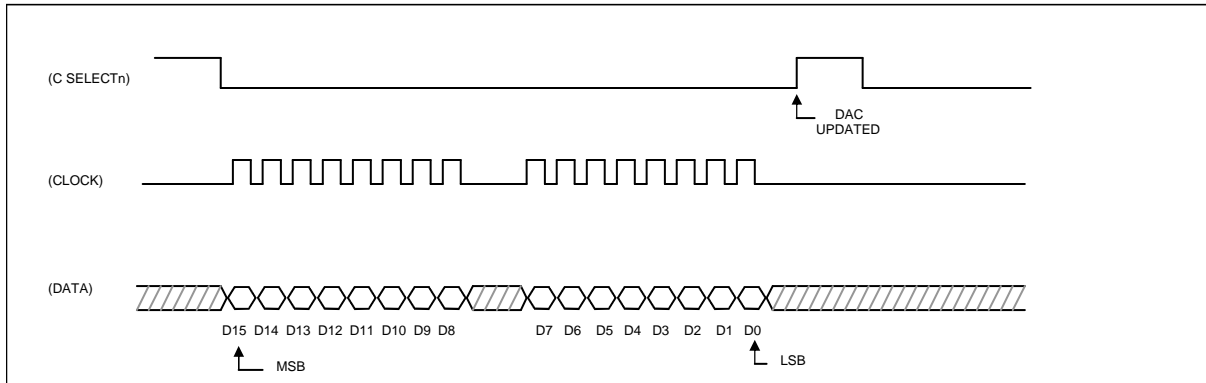


Figure 2. 3-Wire Interface Timing Diagram

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK Frequency	f _{CLK}				10	MHz
CLOCK Pulse Width High	t _{CH}		45			ns
CLOCK Pulse Width Low	t _{CL}		45			ns
CS _n Low to CLOCK High Setup	t _{CSS0}		45			ns
CS _n High to CLOCK High Setup	t _{CSS1}		45			ns
CLOCK High to CS _n Low Hold	t _{CSH0}		30			ns
CLOCK High to CS _n High Hold	t _{CSH1}		45			ns
DATA to CLOCK High Setup	t _{DS}		40			ns
DATA to CLOCK High Hold	t _{DH}		0			ns
VDD High to CS _n Low (power-up delay)				20		μs

SD-SERIES — CONT.

FM Coil Driver (SG Option)

Voltage	± 10 V
Current	± 100 mA
Input Impedance	1 k-Ohms
Sensitivity (Note 3)	± 2.5 MHz/V
Frequency Deviation	± 25 MHz

Note: 1. Optional 1mS Tuning Speeds Available.
 2. Some YIG devices require higher voltages - Check with factory.
 3. FM Coil Sensitivity Adjustment Available. Sensitivity Stated is Average Over Frequency Range.

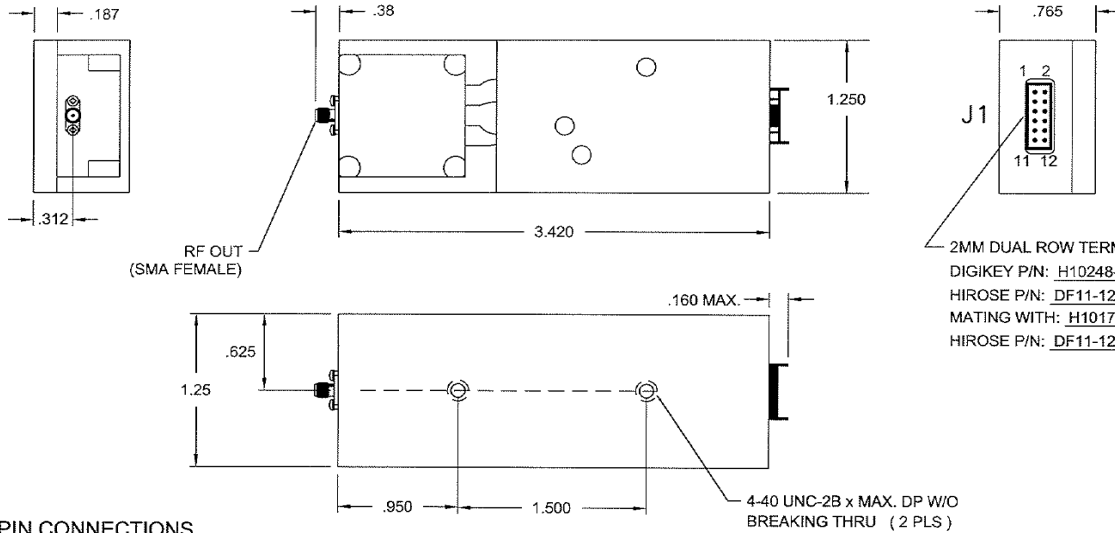
PERFORMANCE SPECIFICATIONS

Permanent Magnet YIG Oscillators with Positive Input Serial Drivers (0° C to +65° C)

Model Number	Frequency GHz	Accuracy (MHz) *	Current +12 V (mA)	Current -12 V (mA)	Outline Drawing	Outline Drawing (SG Option)
Bi-Polar						
MLPM-0204SD	2-4	+/- 10	265	165	61-105	61-105
MLPM-0305SD	3-5	+/- 10	265	165	61-105	61-105
MLPM-0406SD	4-6	+/- 10	265	165	61-105	61-105
MLPM-0507SD	5-7	+/- 10	265	165	61-105	61-105
MLPM-0608SD	6-8	+/- 10	265	165	61-105	61-105
MLPM-0709SD	7-9	+/- 10	265	165	61-105	61-105
MLPM-0810SD	8-10	+/- 10	265	165	61-105	61-105
MLPM-0911SD	9-11	+/- 10	265	165	61-105	61-105
MLPM-1012SD	10-12	+/- 10	265	165	61-105	61-105
MLPM-1113SD	11-13	+/- 10	265	165	61-105	61-105
MLPM-1214SD	12-14	+/- 10	265	165	61-105	61-105

Model Number	Frequency GHz	Accuracy (MHz) *	Current +15 V (mA)	Current -15 V (mA)	Outline Drawing	Outline Drawing (SG Option)
Ultra-Wide Tuning Range						
MLPW-0812SD	8-12	+/- 15	315	215	61-106	61-106
MLPW-1014SD	10-14	+/- 15	315	215	61-106	61-106
MLPW-1418SD	14-18	+/- 15	315	215	61-106	61-106
MLPW-1822SD	18-22	+/- 15	315	215	61-106	61-106

* Accuracy includes frequency drift and linearity errors over the temperature range.

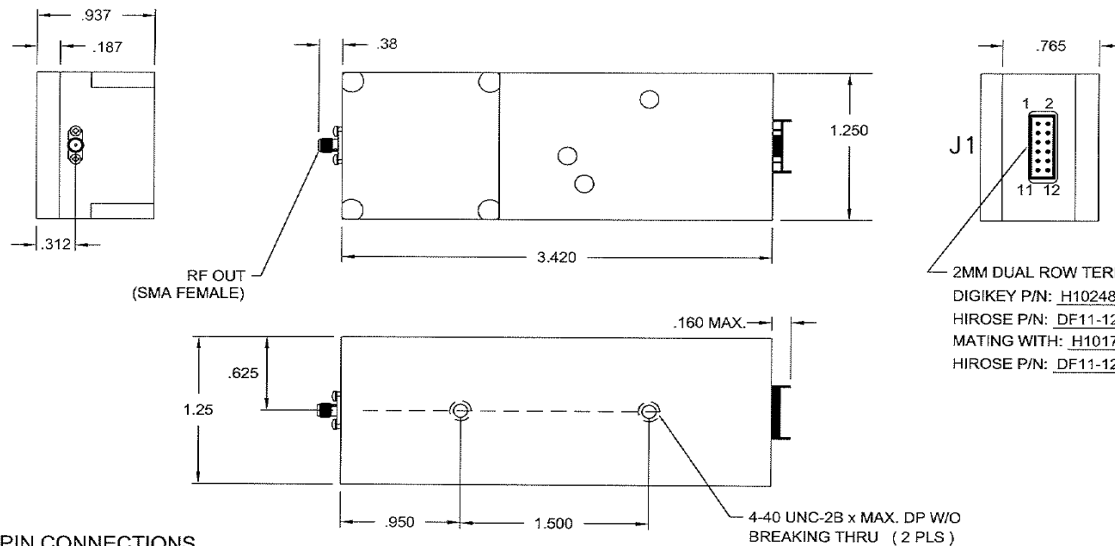


J1 - PIN CONNECTIONS

PIN NO	FUNCTION
1	CLOCK
2	DATA IN
3	CSELECTn
4	GROUND
5	-V SUPPLY
6	+V SUPPLY
7	HTR + or N/C
8	HTR - or N/C
9	FM + or FM V
10	FM - or FM GND
11	N/C
12	N/C

REV	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ARE: FRACTIONS .XX ±.02 ANGLES .XX ±.010		CONTRACT NO.			MICRO LAMBDA WIRELESS, INC.			
MATERIAL		APPROVALS	DATE		OSC. 1.00" W/16BIT SERIAL DRIVER			
FINISH		DRAWN N.NGUYEN	2/23/09	SIZE	CAGE	DWG. NO.	REV.	
DO NOT SCALE DRAWING		ENGR DS	5/15/09		ORN63	61 - 105		
		MANUF		SCALE		SHEET		
		Q.A.						



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REV	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ARE: FRACTIONS .XX ±.02 ANGLES .XX ±.010		CONTRACT NO.			MICRO LAMBDA WIRELESS, INC.			
MATERIAL		APPROVALS	DATE		OSC. 1.25" W/16BIT SERIAL DRIVER			
FINISH		DRAWN N.NGUYEN	2/23/09	SIZE	CAGE	DWG. NO.	REV.	
DO NOT SCALE DRAWING		ENGR DS	5/15/09		ORN63	61 - 106		
		MANUF		SCALE		SHEET		
		Q.A.						